

**DDR SDRAM**
**8M x 16 Bit x 4 Banks**
**Double Data Rate SDRAM**
**Features**

- Double-data-rate architecture, two data transfers per clock cycle
- Bi-directional data strobe (DQS)
- Differential clock inputs (CLK and  $\overline{\text{CLK}}$ )
- DLL aligns DQ and DQS transition with CLK transition
- Four bank operation
- CAS Latency : 2.5, 3, 4
- Burst Type : Sequential and Interleave
- Burst Length : 2, 4, 8
- All inputs except data & DM are sampled at the rising edge of the system clock (CLK)
- Data I/O transitions on both edges of data strobe (DQS)
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Data mask (DM) for write masking only
- $V_{DD} = 2.5V \pm 0.2V$ ,  $V_{DDQ} = 2.5V \pm 0.2V$
- 7.8us refresh interval
- Auto & Self refresh
- 2.5V I/O (SSTL\_2 compatible)

**Ordering Information**

Product ID	Max Freq.	$V_{DD}$	Package	Comments
CT53V32M1601A-5T	200MHz (DDR400)	2.5V	66 pin TSOPII	Pb-free
CT53V32M1601A-6T	166MHz (DDR333)			

如需获取完整版规格书  
请联系我司岳经理  
电话：18138426570  
微信二维码如下：



Linda

