512Mx8, 256Mx16 4Gb DDR3 SDRAM

FEBRUARY 2018

FEATURES

- Standard Voltage: V_{DD} and V_{DDQ} = 1.5V ± 0.075V
- Low Voltage (L): V_{DD} and V_{DDQ} = 1.35V + 0.1V, -0.067V
  - Backward compatible to 1.5V
- High speed data transfer rates with system frequency up to 1066 MHz
- 8 internal banks for concurrent operation
- 8n-Bit pre-fetch architecture
- Programmable CAS Latency
- Programmable Additive Latency: 0, CL-1,CL-2
- Programmable CAS WRITE latency (CWL) based on tCK
- Programmable Burst Length: 4 and 8
- Programmable Burst Sequence: Sequential or Interleave
- BL switch on the fly
- Auto Self Refresh(ASR)
- Self Refresh Temperature(SRT)
- Refresh Interval:
  7.8 us (8192 cycles/64 ms) Tc= -40°C to 85°C
  3.9 us (8192 cycles/32 ms) Tc= 85°C to 105°C
- Partial Array Self Refresh
- Asynchronous RESET pin
- TDQS (Termination Data Strobe) supported (x8 only)
- OCD (Off-Chip Driver Impedance Adjustment)
- Dynamic ODT (On-Die Termination)
- Driver strength : RZQ/7, RZQ/6 (RZQ = 240 Ω)
- Write Leveling
- Up to 200 MHz in DLL off mode
- Operating temperature:
  Commercial (T_C = 0°C to +95°C)
  Industrial (T_C = -40°C to +95°C)
  Automotive, A1 (T_C = -40°C to +95°C)
  Automotive, A2 (T_C = -40°C to +105°C)

OPTIONS

- Configuration:
  512Mx8
  256Mx16
- Package:
  96-ball BGA (9mm x 13mm) for x16
  78-ball BGA (9mm x 10.5mm) for x8

ADDRESS TABLE

Parameter	512Mx8	256Mx16
Row Addressing	A0-A15	A0-A14
Column Addressing	A0-A9	A0-A9
Bank Addressing	BA0-2	BA0-2
Page size	1KB	2KB
Auto Precharge Addressing	A10/AP	A10/AP
BL switch on the fly	A12/BC#	A12/BC#

SPEED BIN

Speed Option	HA	HD	HP	HB	Units
JEDEC Speed Grade	DDR3-1333H	DDR3-1600K	DDR3-1866M	DDR3-2133N	
CL-nRCD-nRP	9-9-9	11-11-11	13-13-13	14-14-14	tCK
tRCD,tRP(min)	13.5	13.75	13.91	13.09	ns

Note:Faster speed options are backward compatible to slower speed options.

如需获取完整版规格书
请联系我司岳经理
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Linda