

FEATURES

- Standard Voltage: V_{DD} and $V_{DDQ} = 1.5V \pm 0.075V$
- Low Voltage (L): V_{DD} and $V_{DDQ} = 1.35V + 0.1V, -0.067V$
-Backward compatible to 1.5V
- High speed data transfer rates with system frequency up to 933 MHz
- 8 internal banks for concurrent operation
- 8n-Bit pre-fetch architecture
- Programmable CAS Latency
- Programmable Additive Latency: 0, CL-1, CL-2
- Programmable CAS WRITE latency (CWL) based on tCK
- Programmable Burst Length: 4 and 8
- Programmable Burst Sequence: Sequential or Interleave
- BL switch on the fly
- Auto Self Refresh(ASR)
- Self Refresh Temperature(SRT)
- Refresh Interval:
 - 7.8 us (8192 cycles/64 ms) $T_c = -40^{\circ}C$ to $85^{\circ}C$
 - 3.9 us (8192 cycles/32 ms) $T_c = 85^{\circ}C$ to $105^{\circ}C$
- Partial Array Self Refresh
- Asynchronous RESET pin
- OCD (Off-Chip Driver Impedance Adjustment)
- Dynamic ODT (On-Die Termination)
- Driver strength : RZQ/7, RZQ/6 (RZQ = 240 Ω)
- Write Leveling
- Up to 200 MHz in DLL off mode
- Operating temperature:
 - Commercial ($T_c = 0^{\circ}C$ to $+95^{\circ}C$)
 - Industrial ($T_c = -40^{\circ}C$ to $+95^{\circ}C$)
 - Automotive, A1 ($T_c = -40^{\circ}C$ to $+95^{\circ}C$)
 - Automotive, A2 ($T_c = -40^{\circ}C$ to $+105^{\circ}C$)

OPTIONS

- Configuration:
512Mx16(dual die)
- Package:
96-ball BGA (9mm x 13mm)

Parameter	512Mx16
Row Addressing	A0-A14
Column Addressing	A0-A9
Bank Addressing	BA0-2
Ranks	2
Page size	2KB
Auto Precharge Addressing	A10/AP
BL switch on the fly	A12/BC#

ADDRESS TABLE
SPEED BIN

Speed Option	HR	HP	Units
JEDEC Speed Grade	DDR3-1600K	DDR3-1866M	
CL-nRCD-nRP	11-11-11	13-13-13	tCK
tRCD,tRP(min)	13.75	13.91	ns

Note:Faster speed options are backward compatible to slower speed options.

如需获取完整版规格书
请联系我司岳经理
电话：18138426570
微信二维码如下：

