# Commercial and Industrial Mobile LPDDR3 4Gb / 8Gb(DDP) SDRAM

## Features

- **JEDEC LPDDR3 Compliant**
  - Low Power Consumption
  - 8n Prefetch Architecture and BL8 only
- **Signal Integrity**
  - Configurable DS for system compatibility
  - Configurable On-Die Termination[1]
  - ZQ Calibration for DS/ODT impedance accuracy via external ZQ pad (240Ω± 1%)
- **Training for Signals' Synchronization**
  - DQ Calibration offering specific DQ output patterns
  - CA Training
  - Write Leveling via MR settings [2]
- **Data Integrity**
  - DRAM built-in Temperature Sensor for Temperature Compensated Self Refresh (TCSR)
  - Auto Refresh and Self Refresh Modes
- **Power Saving Modes**
  - Deep Power Down Mode (DPD)
  - Partial Array Self Refresh (PASR)
  - Clock Stop capability during idle period
- **HSUL12 interface and Power Supply**
  - VDD1= 1.70 to 1.95V
  - VDD2/VDDQ/VDDCA = 1.14 to 1.3V

## Options

- **Speed Grade (DataRate/Read Latency)**
  - 1866 Mbps / RL=14
  - 1600 Mbps / RL=12
- **Temperature Range (*Tc*)**
  - Commercial Grade = - 25℃ to + 85℃
  - Industrial Grade = - 40℃ to + 85℃

## Programmable functions

- **RON (Typical:34.3/40/48/60/80)**
- **RON (PD34.3_PU40 / PD40_PU48 / PD34.3_PU48)**
- **RTT (120/240)**
- **RL/WL Select (Set A / Set B)[3]**
- **nWRE ( nWR≦9 / nWR>9)**
- **PASR (bank/segment)**

## Packages / Density information

**Lead-free RoHS compliance and Halogen-free**

| FBGA Package | Width x Length x Height (mm) | Ball pitch (mm) |
|---|---|---|
| 168b PoP | 12.00 x 12.00 x 0.80 | 0.50 |
| 178b | 10.50 x 11.50 x 0.80 | 0.65/0.80 Mixed |
| 216b PoP | 12.00 x 12.00 x 0.80 | 0.40 |

**Density, Signals and Addressing**

| Items | 4Gb (SDP) | | 8Gb (DDP) | |
|---|---|---|---|---|
| | X16 | X32 | X16 | X32 |
| $\overline{CS}$ | $\overline{CS}$ | | $\overline{CS}$[1:0] | |
| CK/$\overline{CK}$/CKE | CK / $\overline{CK}$ / CKE | | CK / $\overline{CK}$ / CKE[1:0] | |
| DQ | [15:0] | [31:0] | [15:0] | [31:0] |
| DQS/DM | [1:0] / [1:0] | [3:0] / [3:0] | [1:0] / [1:0] | [3:0] / [3:0] |
| CA | CA[9:0] | | | |
| Bank Addr. | BA[2:0] | | | |
| Row Addr.[4] | R[13:0] | | | |
| Column Addr.[4] | C[10:0] | C[9:0] | C[10:0] | C[9:0] |
| tREFI | 3.9μs (Tc≦ 85oC) | | | |

NOTE 1 Depending on ballout, ODT pin may be NOT supported so ODT die pad is connected to Vss inside the package.
NOTE 2 Write Leveling DQ feedback on all DQs
NOTE 3 LPDDR3-1866 only supports Set A.
NOTE 4 Row and Column Addresses values on the CA bus that are not used are "don't care."

如需获取完整版规格书
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